**IN THE CLAIMS:**

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A complementary metal oxide semiconductor (CMOS) device structure comprising:

an N-type field effect transistor (NFET) gate conductor and a P-type field effect transistor (PFET) gate conductor formed on a substrate;

[[a]] first ~~spacer~~ spacers formed on sidewalls of said NFET gate conductor and said PFET gate conductor;

first impurity source/drain implant regions formed, in said substrate, substantially adjacent to outer edges of said first ~~spacer~~ spacers, formed on said sidewalls of said NFET gate conductor;

[[a]] second ~~spacer~~ spacers formed on outer sidewalls of said first ~~spacer~~ spacers, said first spacers being formed on said sidewalls of said PFET gate conductor~~, which is formed on said sidewalls of said PFET gate conductor~~;

an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers; and

second impurity source/drain implant regions, formed in said substrate, substantially adjacent to outer edges of said second ~~spacer~~ spacers formed on said outer sidewalls of said first ~~spacer, which is~~ spacers, formed on said sidewalls of said PFET gate conductor.

2. (Currently Amended) The CMOS device structure according to claim 1, further comprising:

an oxide layer formed directly on tops and said sidewalls of said NFET gate conductor and said PFET gate conductor, and directly on areas of said substrate not covered by said NFET gate conductor and said PFET gate conductor.

3-6. (Canceled).

7. (Previously Presented) The CMOS device structure according to claim 2, further comprising:

silicide regions formed on exposed areas of said oxide layer over said substrate and tops of said NFET gate conductor and said PFET gate conductor.

8. (Canceled).

9. (Previously Presented) The CMOS device structure according to claim 1, wherein a first impurity of said first impurity source/drain implant regions comprises arsenic.

10-11. (Canceled).

12. (Previously Presented) The CMOS device structure according to claim 1, wherein a second impurity of said second impurity source/drain implant regions comprises boron.

13. (Currently Amended) The CMOS device structure according to claim [[3]] 1, wherein said ~~oxide~~ etch stop layer comprises a low temperature oxide.

14. (Currently Amended) The CMOS device structure according to claim 1, wherein said first ~~spacer~~ spacers and said second ~~spacer~~ spacers comprise nitride films.

15-26. (Canceled).

27. (Currently Amended) The CMOS device structure according to claim [[4]] 7, wherein said silicide regions comprise cobalt silicide.

28-36. (Cancelled).

37. (New) A complementary metal oxide semiconductor (CMOS) device structure comprising:

an N-type field effect transistor (NFET) gate conductor and a P-type field effect transistor (PFET) gate conductor formed on a substrate;

first spacers formed on sidewalls of said NFET gate conductor and said PFET gate conductor;

first impurity source/drain implant regions formed, in said substrate, substantially adjacent to outer edges of said first spacers, formed on said sidewalls of said NFET gate conductor;

second spacers formed on outer sidewalls of said first spacers, said first spacers being formed on said sidewalls of said PFET gate conductor;

an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers,

wherein said etch stop layer comprises a low temperature oxide; and

second impurity source/drain implant regions, formed in said substrate, substantially adjacent to outer edges of said second spacers formed on said outer sidewalls of said first spacers, formed on said sidewalls of said PFET gate conductor.